AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Original) A clock converter for synchronizing the phase of a phase locked loop (PLL) feedback signal output from voltage controlled oscillating means with the phase of an input signal using phase detector means, to output a clock signal of a predetermined frequency, comprising:

voltage controlled oscillating means outputting a positive feedback signal for a positive feedback loop from one output terminal of buffer means forming a portion of the positive feedback loop, which uses voltage controlled phase shifting means, and outputs the PLL feedback signal from another output terminal of the buffer means.

2. (Original) The clock converter according to Claim 1, wherein the buffer means of the voltage controlled oscillating means further comprises an ECL (emitter coupled logic) differential amplifying circuit.

3. (Original) The clock converter according to Claim 1, wherein:

the PLL feedback signal output from the buffer means is fed back to the phase detector means through signal transmitting means for adjusting impedance; and

feedback frequency dividing means for dividing the frequency of the PLL feedback signal.

4. (Original) The clock converter according to Claim 3, wherein:

in the signal transmitting means, the PLL feedback signal supplied from the buffer means is supplied to a first connection point between a first resistor and a second resistor among first to third resistors connected in series between a power source and a ground;

a second connection point between the second resistor and third resistor is connected to the ground through a first capacitor;

the first connection point is connected to a first input terminal of a differential ECL amplifier in the feedback frequency dividing means; and

the second connection point is connected to a second input terminal of the differential ECL amplifier in the feedback frequency dividing means.

5. (Original) The clock converter according to Claim 3, wherein:

in the signal transmitting means, the PLL feedback signal supplied from the buffer means is supplied to a first connection point between the first resistor and the second resistor among first to third resistors connected in series between a power source and a ground through a second capacitor;

a second connection point between the second resistor and third resistor is connected to the ground through a first capacitor;

the first connection point is connected to a first input terminal of a differential CMOS amplifier in the feedback frequency dividing means; and

the second connection point is connected to a second input terminal of the differential CMOS amplifier in the feedback frequency dividing means.

6. (Original) The clock converter according to Claim 4, wherein, when the resistance value of the second resistor is R_M, and the resistance values of the first and the third resistors connected to both ends of the second resistor are R_H and R_L, respectively, then $R_H >> R_M$ and $R_L >> R_M$.

7. (Original) The clock converter according to Claim 4, wherein an output terminal of the differential amplifying circuit forming the buffer means of the voltage controlled oscillating means is connected to a termination resistor with a resistance value larger than that of the output impedance of the differential amplifying circuit.

8. (Withdrawn)

9. (Withdrawn)

10. (Withdrawn)

11. (Withdrawn)

12. (Original) The clock converter according to Claim 5, wherein, when the resistance value of the second resistor is R_M, and the resistance values of the first and the third resistors connected to both ends of the second resistor are R_H and R_L, respectively, then $R_H >> R_M$ and $R_L >> R_M$.

13. (Withdrawn)

14. (Withdrawn)

15. (Withdrawn)